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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,870	01/18/2002	Zhongming Shi	BP1985	1734
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GARLICK HARRISON & MARKISON LLP P.O. BOX 160727 AUSTIN, TX 78716-0727			PERILLA, JASON M	
			ART UNIT	PAPER NUMBER
			2638	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/052,870

Applicant(s)

SHI ET AL.

Examiner

Jason M. Perilla

Art Unit

26348

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-32 are pending in the instant application.

Specification

2. The specification is objected to because the "Brief Description of the Drawings" section does not include figures 7 and 8.

Claim Objections

3. Claim 1-32 are objected to because of the following informalities:

Regarding claim 1, in line 4, "controlcontrol" should be replaced by --control--, in line 5, "the received radio frequency communications signal" is lacking antecedent basis, in line 8, "the output" should be replaced by --an output--, and, in line 10, "converting received" should be replaced by --converting the received--.

Regarding claim 2, in line 2, "controlcontrol" should be replaced by --control--.

Regarding claim 4, in line, "to receiver port" should be replaced by --to a receiver port--and "transceiver and" should be replaced by --transceiver port and--, and, in line 3, "LO" should be replace by --local oscillator (LO), "RF" should be replaced by --radio frequency (RF), and "the desired RF channel" is lacking antecedent basis.

Regarding claim 6, in line 2, "RF" should be replaced by --radio frequency (RF)--.

Regarding claim 7, in line 1, "RC" should be replaced by --resistive capacitive (RC)--, and, in lines 2-3, "the on-chip channel selection low pass filters" is lacking antecedent basis.

Regarding claim 8, in line 5, "RF" should be replaced by --radio frequency (RF)--, and, in line 7, "DC" should be replaced by --direct current (DC)--.

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Regarding claim 14, in line 3, "LO" should be replaced by --local oscillator (LO)--.

Regarding claim 15, in line 2, "a DC offset" should be replaced by "the DC offset".

Regarding claim 18, in line 1, "RC" should be replaced by --resistive capacitive (RC)--.

Regarding claim 19, in line 5, "the LO" should be replaced by --a local oscillator (LO)-- and "RF" should be replaced by --radio frequency (RF)--.

Regarding claim 20, in line 2, "the DC offset" should be replaced by --a direct current (DC) offset--.

Regarding claim 23, in line 2, "the received signals and interference" is lacking antecedent basis.

Regarding claim 29, in line 7, "DC" should be replaced by --direct current (DC)--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 24-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 24, one skilled in the art is unable to determine the meaning of signal-to-signal and interference power levels. The body of the specification does not enable one skilled in the art to set an amplification based upon a signal-to-signal ratio because the meaning of a signal-to-signal ratio is not described in the specification such that one would be enabled to make or use it.

Regarding claim 25, the claim is rejected for the same reasons as applied to claim 24 above.

Regarding claim 26, the claim is rejected as being based upon a rejected parent claim.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 27 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 27, the claim is indefinite because one is unable to determine the meaning of "the desired frequency". One is unable to determine if "the desired frequency" is related to the frequency of the information from the pilot signal or an expected frequency of the received RF signal, and it makes the claim indefinite.

Regarding claim 28, the claim is rejected as being based upon a rejected parent claim.

Claim Rejections - 35 USC § 102

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8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 8, 13, 14-17, and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Baldwin et al (US 6560448; hereafter "Baldwin").

Regarding claim 8, Baldwin discloses by figure 1 a transceiver (abstract), comprising; a transceiver port (247, 249) for receiving and transmitting radio frequency communication signals; an automatic frequency control circuit (231) for adjusting the center frequency of a received RF signal; circuitry for down converting (265, 267) the received RF signal; and circuitry (284, 293, 295, 269, and 271) for removing a DC offset and low frequency interference (col. 6, lines 42-60; col. 10, lines 13-33).

Regarding claim 13, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses that the automatic frequency control circuitry comprises signal generation circuitry (fig. 2, refs. 229, 227) that provides quadrature phase shift keyed or in-phase and quadrature signals.

Regarding claim 14, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses that the automatic frequency control circuitry (fig. 2, refs. 229, 231 and 227) receives base band quadrature signals output from the local

oscillator (fig. 2, ref. 229) and produces an adjusted LO signal (fig. 2, output from ref. 227) output from a local oscillator.

Regarding claim 15, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses filter circuitry for removing a DC offset (fig. 2, ref. 269, 271). The filters 269 and 271 receive feedback from the logic controller via control lines IDC_{OFF} and QDC_{OFF} to remove a DC offset.

Regarding claim 16, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses filter circuitry for removing low frequency interference (fig. 2, ref. 269, 271). Filters 269 and 271 are low pass filters (LPF).

Regarding claim 17, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses an up converter (fig. 2, ref. 223, 225) for up converting base band signals to radio frequency signals for transmission from the transceiver port (fig. 2, ref. 247, 249).

Regarding claim 19, Baldwin discloses the limitations of claim 19 as applied to claim 8 above.

Regarding claim 20, Baldwin discloses the limitations of claim 19 as applied above. Further, Baldwin discloses removing a DC offset (col. 6, lines 42-60; col. 10, lines 13-33).

Regarding claim 21, Baldwin discloses the limitations of claim 19 as applied above. Further, Baldwin discloses removing low frequency interference via low pass filters (fig. 2, refs. 269, 271).

Regarding claim 22, Baldwin discloses the limitations of claim 19 as applied above. Further, Baldwin discloses sensing a power level of the received signals (col. 10, lines 13-18) so that a gain of the received signals could be adjusted by the feedback signal G_{ADJ} (fig. 2).

Regarding claim 23, Baldwin discloses the limitations of claim 19 as applied above. Further, Baldwin discloses sensing a power level and interference of the received signals (col. 10, lines 13-18) so that a gain of the received signals could be adjusted by the feedback signal G_{ADJ} (fig. 2). It is necessary to receive any interference coupled with the received signal while sensing the power level of the received signal because any interference is superimposed upon the received signal.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin.

Regarding claim 18, Baldwin discloses the limitations of claim 8 as applied above. Further, Baldwin discloses calibration circuitry (fig. 2, ref. 284) for automatically tuning the on chip filters (fig. 2, ref. 269, 271). The filters 269 and 271 receive feedback from the logic controller via control lines IDC_{OFF} and QDC_{OFF} to remove a DC offset. Baldwin does not explicitly disclose that the filters (269, 271) comprise resistive capacitive elements. However, as understood by one having ordinary skill in the art,

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filters comprise resistive and capacitive elements. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the calibration circuitry (fig. 2, ref. 284) would calibrate resistive capacitive filters (269, 271) via the control lines IDC_{OFF} and QDC_{OFF} .

12. Claims 9, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin in view of Shi (US 2003/0064695).

Regarding claim 9, Baldwin discloses the limitations of claim 8 as applied above. Baldwin does not disclose dual received signal indication circuits, which dual received signal indicator circuits are for measuring received signal power and received signal and interference power. However, Shi teaches the use of received signal strength indicators for the proper adjustment of variable gain amplifiers. The variable gain amplifiers (fig. 1, refs. 261 and 273) of Baldwin are controlled by the logic controller (fig. 1, ref. 284), but Baldwin does not explicitly provide for the means used to determine the amount of gain adjustment needed. Shi teaches that the received signal strength indicators (fig. 2, refs. 218 and 220) are used to adjust variable gain amplifiers (fig. 2, ref. 220 and 210; para. 0013, 0034-0036). Shi teaches that the received signal strength indicators and the gain adjustment block are advantageously utilized to maintain the variable gain amplifiers operating in their linear range while maximizing the signal to noise ratio (para. 0035). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize received signal strength indicators as taught by Shi in the transceiver of Baldwin because they could be used to maximize the signal to noise ratio while maintaining the variable gain amplifiers in a linear range of operation.

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In the transceiver of Baldwin in view of Shi, two received signal strength indicators (RSSI) would be applied, as taught by Shi. One RSSI unit would be utilized to measure the received signal and power to adjust the gain of the first variable gain amplifier (fig. 1, ref. 261) of Baldwin via the logic controller, and a second RSSI unit would be utilized to measure the received signal power to adjust the gain of the second variable gain amplifier (fig. 1, ref. 273, 275) of Baldwin via the logic controller.

Regarding claim 24, Baldwin discloses the limitation of claim 19 as applied above. Baldwin does not explicitly disclose that a first amplification level is based upon a ratio of signal to noise and interference levels. However, Shi teaches the use of received signal strength indicators for the proper adjustment of variable gain amplifiers. The variable gain amplifiers (fig. 1, refs. 261 and 273) of Baldwin are controlled by the logic controller (fig. 1, ref. 284), but Baldwin does not explicitly provide for the means used to determine the amount of gain adjustment needed. Shi teaches that the received signal strength indicators (fig. 2, refs. 218 and 220) are used to adjust variable gain amplifiers (fig. 2, ref. 220 and 210; para. 0013, 0034-0036). Shi teaches that the received signal strength indicators and the gain adjustment block are advantageously utilized to maintain the variable gain amplifiers operating in their linear range while maximizing the signal to noise ratio (para. 0035). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize received signal strength indicators as taught by Shi in the transceiver of Baldwin because they could be used to maximize the signal to noise ratio while maintaining the variable gain amplifiers in a linear range of operation. In the transceiver of Baldwin in

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view of Shi, two received signal strength indicators (RSSI) would be applied, as taught by Shi. One RSSI unit would be utilized to measure the received signal and power to adjust the gain of the first variable gain amplifier (fig. 1, ref. 261) of Baldwin via the logic controller, and a second RSSI unit would be utilized to measure the received signal power to adjust the gain of the second variable gain amplifier (fig. 1, ref. 273, 275) of Baldwin via the logic controller. Therefore, in the transceiver of Baldwin in view of Shi, a first amplification level (the gain of the variable gain amplifier fig. 2, ref. 273, 275) would be based upon a signal to noise and interference power level because the RSSI indicator would measure a signal to noise and interference level to accordingly adjust the power level of the variable gain amplifier.

Regarding claim 25, Baldwin in view of Shi disclose the limitations of claim 24 as applied above. Further, in the transceiver of Baldwin in view of Shi, a second amplification level (the gain of the variable gain amplifier fig. 2, ref. 261) would be based upon a signal to noise and interference power level because the RSSI indicator would measure a signal to noise and interference level to accordingly adjust the power level of the variable gain amplifier.

Regarding claim 26, Baldwin in view of Ichihara disclose the limitations of claim 25 as applied above. Further, the purpose of the adjustment of the amplification of the variable gain amplifiers of Baldwin is to provide the correct amount of amplification. Therefore, it would have been obvious that the first and second amplification levels, collectively, would provide the correct amount of amplification for the transceiver.

13. Claims 10-12 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin in view of Ichihara (US 2002/0047744).

Regarding claim 10, Baldwin discloses the limitations of claim 8 as applied above. Baldwin discloses variable gain amplification circuitry (fig. 1, ref. 273, 275) but does not explicitly disclose high pass variable gain amplification circuitry. However, Ichihara teaches the use of variable gain amplifiers coupled with high pass filters to reduce DC offset (fig. 7). Ichihara teaches that a plurality of high pass (C-cut) filters each coupled with a variable gain amplifier connected in series can remove a DC offset while uniformly amplifying a signal (para. 0014-0017, 0068). Further, Ichihara teaches that the DC blocking gain control circuit shown in figure 7 can be adjusted evenly and gradually with the plurality of variable gain amplifiers to suppress any sudden change in transient (DC) voltage (para. 0080). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the high pass (C-cut) filter and variable gain arrangement as taught by Ichihara (fig. 7) in place of the variable gain amplifiers of Baldwin because they could be advantageously be used to remove any DC offset while gradually and evenly amplifying the received signal.

Regarding claim 11, Baldwin in view of Ichihara disclose the limitations of claim 10 as applied above. Further, in the transceiver of Baldwin in view of Ichihara, the transceiver includes first high pass filter and variable amplifier (Ichihara; fig. 7, refs. 108, 102), second high pass filter and variable amplifier (fig. 7, refs. 109, 103), and third high pass filter and variable amplifier (fig. 7, refs. 110, 104).

Regarding claim 12, Baldwin in view of Ichihara disclose the limitations of claim 11 as applied above. Further, in the transceiver of Baldwin in view of Ichihara, the transceiver includes first high pass filter and variable amplifier (Ichihara; fig. 7, refs. 108, 102), second high pass filter and variable amplifier (fig. 7, refs. 109, 103), and third high pass filter and variable amplifier (fig. 7, refs. 110, 104).

Regarding claim 29, Baldwin in view of Ichihara disclose the limitations of claim 29 as applied to claim 10 above.

Regarding claim 30, Baldwin in view of Ichihara disclose the limitations of claim 29 as applied above. Further, Baldwin discloses by figure 2 that the frequency control circuitry includes circuitry (231) for measuring a center channel frequency (257) and for determining a difference between the measured center channel frequency and a specified center channel frequency (229).

Regarding claim 31, Baldwin in view of Ichihara disclose the limitations of claim 31 as applied above. Further, Baldwin discloses signal generation circuitry (fig. 2, ref. 209) for generating quadrature phase shift keyed signals (fig. 2, output of 211 and 213).

Regarding claim 32, Baldwin in view of Ichihara disclose the limitations of claim 32 as applied above. Further, Baldwin discloses a mixer (fig. 2, ref. 227) for producing local oscillator output signals at a specified frequency. The specified frequency is the particular frequency of the carrier of the received signals.

14. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin in view of Ichihara, and in further view of Shi.

Regarding claim 1, Baldwin discloses a transceiver by figure 2, comprising: a transceiver port (247, 249) for receiving and transmitting high data rate communication signals at radio frequency; automatic frequency control circuitry for adjusting the received radio frequency communication signals to a specified frequency channel (229, 231, and 227); down conversion circuitry (265, 267) coupled to the transceiver port coupled to receive the output of the automatic frequency control circuitry, the down conversion circuitry for down converting received radio frequency communication signals to base band frequency communication signals (abstract); low pass filtering circuitry (269, 271) coupled to receive down converted frequency signals from the down conversion circuitry, the low pass filtering circuitry for removing a DC offset and low frequency interference (col. 6, lines 42-60; col. 10, lines 13-33), and variable gain amplification circuitry (273, 275). Baldwin does not explicitly disclose (a) high pass filtering circuitry coupled to receive down converted frequency signals, the high pass filtering circuitry for filtering interference signals that are at a frequency range that is higher than a specified frequency channel (the down converted base band channel) or (b) dual received signal strength indication circuits for measuring power levels of signal and interference. However, Ichihara teaches the use of variable gain amplifiers coupled with high pass filters to reduce DC offset (fig. 7). Ichihara teaches that a plurality of high pass (C-cut) filters each coupled with a variable gain amplifier connected in series can remove a DC offset while uniformly amplifying a signal (para. 0014-0017, 0068). Further, Ichihara teaches that the DC blocking gain control circuit shown in figure 7 can be adjusted evenly and gradually with the plurality of variable gain amplifiers to

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suppress any sudden change in transient (DC) voltage (para. 0080). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the high pass (C-cut) filter and variable gain arrangement as taught by Ichihara (fig. 7) in place of the variable gain amplifiers of Baldwin because they could be advantageously be used to remove any DC offset while gradually and evenly amplifying the received signal thus meeting the claimed limitation (a).

Further regarding claim 1, Shi teaches the use of received signal strength indicators for the proper adjustment of variable gain amplifiers. The variable gain amplifiers (fig. 1, refs. 261 and 273) of Baldwin in view of Ichihara are controlled by the logic controller (fig. 1, ref. 284), but Baldwin in view of Ichihara does not explicitly provide for the means used to determine the amount of gain adjustment needed. Shi teaches that the received signal strength indicators (fig. 2, refs. 218 and 220) are used to adjust variable gain amplifiers (fig. 2, ref. 220 and 210; para. 0013, 0034-0036). Shi teaches that the received signal strength indicators and the gain adjustment block are advantageously utilized to maintain the variable gain amplifiers operating in their linear range while maximizing the signal to noise ratio (para. 0035). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize received signal strength indicators as taught by Shi in the transceiver of Baldwin in view of Ichihara because they could be used to maximize the signal to noise ratio while maintaining the variable gain amplifiers in a linear range of operation. In the transceiver of Baldwin in view of Ichihara, and in further view of Shi, two received signal strength indicators (RSSI) would be applied, as taught by Shi. One RSSI unit would be

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utilized to measure the received signal and power to adjust the gain of the first variable gain amplifier (fig. 1, ref. 261) of Baldwin via the logic controller, and a second RSSI unit would be utilized to measure the received signal power to adjust the gain of the second variable gain amplifier (fig. 1, ref. 273, 275) of Baldwin via the logic controller thus meeting the claimed limitation (b).

Regarding claim 2, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 1 as applied above. Further, Baldwin discloses that the automatic frequency control circuitry comprises signal generation circuitry (fig. 2, refs. 229, 227) that provide phase shift keyed or in-phase and quadrature signals.

Regarding claim 3, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 2 as applied above. Further, Baldwin discloses that the phase shift keyed signal generation circuitry (fig. 2, refs. 229, 227) comprises quadrature phase shift keyed or in-phase and quadrature signal generation circuitry.

Regarding claim 4, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 1 as applied above. Further, the local oscillator frequency provided by the phase locked loop frequency generator (fig. 2, refs. 229, 231, and 227) is adjusted to the frequency of the desired RF signal because it is used to downconvert the received RF signal directly to baseband via the mixers (fig. 2, ref. 265 and 267).

Regarding claim 5, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 1 as applied above. Further, Ichihara discloses, as broadly as claimed, that the high pass filtering circuitry and the variable gain amplification circuitry

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are combined to for a high pass filter variable gain amplifier circuit (fig. 7, refs. 109 and 103).

Regarding claim 6, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 1 as applied above. Further, Baldwin discloses an up converter (fig. 2, refs. 223, 225) for converting base band signals to RF signals for transmission from the transceiver.

Regarding claim 7, Baldwin in view of Ichihara, and in further view of Shi disclose the limitations of claim 1 as applied above. Further, Baldwin discloses calibration circuitry (fig. 2, ref. 284) for automatically tuning the on chip filters (fig. 2, ref. 269, 271). The filters 269 and 271 receive feedback from the logic controller via control lines IDC_{OFF} and QDC_{OFF} to remove a DC offset. Baldwin does not explicitly disclose that the filters (269, 271) comprise resistive capacitive elements. However, as understood by one having ordinary skill in the art, filters comprise resistive and capacitive elements. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the calibration circuitry (fig. 2, ref. 284) would calibrate resistive capacitive filters (269, 271) via the control lines IDC_{OFF} and QDC_{OFF} .

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to DC offset removing direct conversion receivers.

U.S. Pat. No. 5949830 to Nakanishi.

U.S. Pat. No. 6127884 to Rishi.

U.S. Pat. No. 6212244 to Davidovici et al.

U.S. Pat. No. 6236848 to Igarashi et al.

U.S. Pub. No. 2001/00550350 to Higure.

U.S. Pub. No. 2001/0022821 to Ichihara.

U.S. Pat. No. 6498929 to Tsurumi et al.

U.S. Pat. No. 6498927 to Kang et al.

U.S. Pub. No. 2003/0025623 to Brueske et al.

U.S. Pat. No. 6748200 to Webster et al.

U.S. Pat. No. 6862439 to Feng.

U.S. Pat. No. 6370370 to Roth et al.

U.S. Pat. No. 6873832 to Shi.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jason M. Perilla
June 13, 2005

jmp



CHIEH M. FAN
PRIMARY EXAMINER